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decoding the input video signal, and performing synchronization in accord with the reference clock, on a frame unit basis, of input side frame reference timing which is obtained on the basis of the time information for synchronization of the input video signal and frame reference timing for output which is obtained by frequency dividing the reference clock; and

an audio signal processing unit, responsive to the clock generator, for decoding a number of the samples of the audio signal for said reference clock, for detecting a difference between periods of said input side frame reference timing and said frame reference timing for output and for correcting the number of samples in accordance with the detected period difference.

23. (New) A digital signal processing device according to claim 22, wherein

the video signal processing unit repetitively outputs a frame if the frame reference timing for output is earlier than the input side frame reference timing, and decimates at least one frame from the output frames if the frame reference timing for output is later than the input side frame reference timing, and

the audio signal processing unit obtains a phase difference period from the input side frame reference timing and the frame reference timing for output, subtracts a number of decoded samples of the audio signal corresponding to the phase difference period from the number of samples of the input audio signal included in one frame period in which the input side frame reference timing is used as a reference, and executes an enlarging or reducing process to the audio signal of the subtracted number of samples, and outputs the audio signal synchronized with the frame reference timing for output, if

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the frame reference timing for output is earlier than the input side frame reference timing, and

the audio signal processing unit obtains the phase difference period from the input side frame reference timing and the frame reference timing for output, and adds a number of samples of the audio signal corresponding to the phase difference period to the number of decoded samples of the input audio signal included in one frame period in which the input side frame reference timing is used as a reference, and executes the enlarging or reducing process to the audio signal of the added number of samples and outputs the audio signal synchronized with the frame reference timing for output if the frame reference timing for output is later than the input side frame reference timing.

24. (New) A digital signal processing device for processing an input digital signal including time reference signal, processing the signal, and obtaining a reproduction signal of a video image and an audio sound, comprising:

a clock signal generator for generating a clock signal asynchronized with the time reference signal;

a frequency dividing unit, coupled to the clock generator, for frequency dividing the clock signal and generating a frame sync signal for output, a clock enable signal for an input process, and a clock enable signal according to an audio operating mode;

a digital interface processor, coupled to the frequency dividing unit, for separating a compressed video signal, an audio signal, auxiliary information, and an input side frame sync signal from the input digital signal in accordance with the clock enable

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signal for the input process from the frequency dividing unit and outputting them;

a video signal processing unit, coupled to the digital interface processor and the frequency dividing unit to receive the compressed video signal and the input side frame sync signal the digital interface processor, and to receive the clock enable signal for the input process and the frame sync signal from the frequency dividing unit, for obtaining a video signal by performing a decoding process, and for executing a synchronizing process to the frame sync signal for output which is outputted from the frequency dividing unit and the input video signal; and

an audio signal processing unit, coupled to the digital interface processor and the frequency dividing unit to receive audio information and the frame sync signal from the digital interface processor, to receive the clock enable signal for the input process and the input side frame sync signal from the frequency dividing unit, the clock enable signal according to the audio operating mode and the frame sync signal for output from the frequency dividing unit, for obtaining the audio signal by performing a signal process, and for outputting the audio signal by the clock enable signal according to the audio operating mode which is outputted from the frequency dividing unit.

25. (New) A digital signal processing device according to claim 24, wherein

the video signal processing unit repetitively outputs a frame if the frame sync signal for output is earlier than the input side frame sync signal, and decimates at least one frame from the output frames if the frame sync signal for output is later than the input side frame sync signal, and

the audio signal processing unit obtains a phase difference period from the

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input side frame sync signal and the frame sync signal for output, subtracts a number of samples of the audio signal corresponding to the phase difference period from the number of decoded samples of the input audio signal included in one frame period in which the input side frame sync signal is used as a reference, and executes an enlarging or reducing process to the audio signal of the subtracted number of samples, and outputs the audio signal synchronized with the frame sync signal for output if the frame sync signal for output is earlier than the input side frame sync signal, and

the audio signal processing unit obtains the phase difference period from the input side frame sync signal and the frame sync signal for output, and adds a number of samples of the audio signal corresponding to the phase difference period to the number of decoded samples of the input audio signal included in one frame period in which the input side frame sync signal is used as a reference, and executes the enlarging or reducing process to the audio signal of the added number of samples, and outputs the audio signal synchronized with the frame sync signal for output if the frame sync signal for output is later than the input side frame sync signal.

26. (New) A digital signal processing device according to claim 22, wherein the video signal and audio signal to which the time information for synchronization has been added are signals which are transmitted and inputted in a format complying with an IEEE1394 standard.

27. (New) A digital signal processing device according to claim 24, wherein the digital signal to which the time reference signal has been added is a signal which is

transmitted and inputted in a format complying with IEEE1394 standard.

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28. (New) A decoder for processing an input audio signal associated with time information for synchronization in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the time information for synchronization and outputting the processed audio signal, comprising:

a frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output on the basis of the reference clock; and

an audio signal processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process of the input audio signal by setting the number of samples of one frame period in which the frame sync signal for output is used as a reference to the number of samples of one frame.

29. (New) A DV decoder for processing a input video signal and an input audio signal associated with time information for synchronization in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the time information for synchronization and outputting the processed video and audio signals, comprising:

a frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output on the basis of the reference clock;

a video signal processing unit, responsive to the frequency dividing unit, for processing the input video signal and outputting the processed video signal synchronized with the frame sync signal for output; and

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an audio signal processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process of the input audio signal so that a number of samples of one frame period in which the frame sync signal for output is used as a reference is equal to the predetermined number of samples.

30. (New) A DV decoder for receiving an input video signal, an input audio signal, auxiliary information, and an input side frame sync signal, processing the input video signal and the input audio signal in accord with a reference clock which is asynchronous with the input side frame sync signal from a clock generator, and outputting the processed video and audio signals, comprising:

a frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output on the basis of the reference clock;

a video processing unit, responsive to the frequency dividing unit, for frame synchronously processing the input video signal and forming the processed video signal synchronized with the frame sync signal for output; and

an audio processing unit, responsive to the frequency dividing unit, for comparing the input side frame sync signal with the frame sync signal for output, setting a number of samples of one frame period by subtracting or adding a number of samples corresponding to a difference between the input side frame sync signal and the frame sync signal for output in accord with an AF_SIZE parameter regarding the number of samples of one frame period obtained from the auxiliary information , and executing a sampling transforming process of the inputted audio signal.

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31. (New) A DV decoder for receiving an input video signal, an input audio signal, auxiliary information, and an input side frame sync signal of a DV format, processing the video signal and the audio signal in accord with a reference clock which is asynchronous with the input side frame sync signal and is outputted from a clock generator, and outputting the processed video and audio signals, comprising:

a separating unit for separating the input video signal and the input audio signal;

a first frequency dividing unit, coupled to the clock generator, for forming an enable signal for an input process on the basis of the reference clock;

a second frequency dividing unit, coupled to the clock generator, for forming an enable signal for an audio signal process on the basis of the reference clock and sampling frequency information of the auxiliary information;

a third frequency dividing unit, coupled to the clock generator, for forming a frame sync signal for output on the basis of the reference clock;

a video signal processing unit, coupled to the first and third frequency dividing unit, for frame synchronously processing the video signal separated by the separating unit and outputting the video signal synchronized with the frame sync signal for output;

an audio signal processor , coupled to the first frequency dividing unit, for writing the audio signal separated by the separating unit into a memory in response to the enable signal for the input process and reading out the audio signal;

a comparator, coupled to the third frequency dividing unit for comparing the input side frame sync signal with the frame sync signal for output; and

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a sampling transform processor, coupled to the second frequency dividing unit for calculating a number of samples corresponding to one frame period of the frame sync signal by adding or subtracting a number of samples of a period corresponding to a difference between the input side frame sync signal and the frame sync signal for output, outputted by the comparator, in accord with an AF_SIZE regarding the number of samples of one frame period from the auxiliary information of the audio signal, executing a transforming process of a number of samples to the audio signal outputted from the audio signal processing unit by performing an enlarging or reducing process based on calculated number of samples o and outputting the audio signal in response to the enable signal for the audio signal process.

32. (New) A DV decoder for processing an input digital signal including video signal, an audio signal and an input side frame sync signal in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the input side frame sync signal and for outputting the processed video and audio signals, comprising:

a frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output and a clock enable signal for an input process on the basis of the reference clock;

an input processing unit, responsive to the frequency dividing unit, for separating and outputting the video signal, the audio signal, and the input side frame sync signal from the input digital signal in response to the clock enable signal for the input process which is outputted from the frequency dividing unit;

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a video processing unit, responsive to the frequency dividing unit, for processing the video signal which is outputted from the input processing unit and forming the video signal synchronized with the frame sync signal for output; and

an audio signal processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process to the audio signal from the input processing unit so that a number of samples of one frame period in which the frame sync signal for output is used as a reference equals to a predetermined number of samples.

33. (New) A DV decoder for processing input digital signal including a compressed video signal, an audio signal, auxiliary information, and an input side frame sync signal in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the input side frame sync signal and outputting the processed video and audio signals, comprising:

a frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output and a clock enable signal for an input process on the basis of the reference clock;

an input processing unit, responsive to the frequency dividing unit, for separating and outputting the compressed video signal, the audio signal, auxiliary information, and an input side frame sync signal from the input digital signal in response to the clock enable signal for the input process which is outputted from the frequency dividing unit;

a video processing unit, responsive to the frequency dividing unit, for decoding the compressed video signal output from the input processing unit in response

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to the clock enable signal for the input process and forming the processed video signal which is frame synchronized with the frame sync signal for output; and

an audio processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process to the audio signal output from the input processing unit by setting a number of samples obtained by adding or subtracting a number of samples corresponding to a difference between the input side frame sync signal and the frame sync signal for output in accord with an AF_SIZE parameter regarding the number of samples of one frame period obtained from the auxiliary information.

34. (New) A digital signal processing device according to claim 24, wherein

the frequency dividing unit comprises a first frequency dividing unit for forming a clock enable signal for an input process on the basis of the reference clock, a second frequency dividing unit for forming a clock enable signal for an audio signal process on the basis of the reference clock and sampling frequency information included in the auxiliary information, and a third frequency dividing unit for forming a frame sync signal for output on the basis of the reference clock, and

the digital interface processor comprises an IEEE interface unit outputting the input side frame sync signal based on the time reference signal in response to the clock enable signal for the input output the first frequency dividing unit and a signal separating unit for separating the audio signal and the compressed video signal from the signal outputted from the IEEE interface unit, and

the video processing unit comprises a video processor for decoding the

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compressed video signal output from the signal separating unit, and a video synchronizer for performing a frame synchronizing process to the video signal outputted from the video processor and forming the video signal synchronized with the frame sync signal for output, and

the audio processing unit comprises a comparator for comparing the input side frame sync signal with the frame sync signal for output, and a sampling transform processor for adding or subtracting the number of samples corresponding to a difference between the input side frame sync signal and the frame sync signal for output in accord with an AF_SIZE parameter regarding a number of samples of one frame period from the auxiliary information, and calculating the number of samples of one frame period in which the frame sync signal for output , and executing a sampling transforming process to the audio signal by performing an enlarging or reducing process by setting the calculated number of samples as the number of samples of one frame period.

35. (New) A decoder according to claim 28, wherein the input audio signal is a signal in an unlocked mode in a DV standard, and the audio processing unit transforms the number of samples into a number of samples which has been predetermined in a locked mode in the DV standard.

36. (New) A DV decoder according to claim 29, wherein the input audio signal is a signal in an unlocked mode in a DV standard, and the audio processing unit transforms a number of samples into the number of samples which has been predetermined in a locked mode in the DV standard.

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37. (New) A DV decoder according to claim 31, wherein the input audio signal is a signal in an unlocked mode in a DV standard, and the sampling transform processor transforms a number of samples into the number of samples which has been predetermined in a locked mode in the DV standard.

38. (New) A recording device comprising:

(a) a decoder for processing an input audio signal input with time information for synchronization in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the time information for synchronization and outputting the processed audio signal, comprising:

a frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output on the basis of the reference clock; and

an audio signal processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process of the input audio signal by setting the number of samples of one frame period in which the frame sync signal for output is used as a reference to the number of samples of one frame;

(b) an MPEG compressing circuit for compressing the processed audio signal outputted from the decoder by MPEG compression and forming compressed data; and

(c) a recording unit for recording the compressed data outputted from the

MPEG compressing circuit.

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39. (New) A recording device comprising:

(a) a DV decoder for processing a input video signal and an input audio signal inputted with time information for synchronization in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the time information for synchronization and outputting the processed video and audio signals, comprising:

a frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output on the basis of the reference clock;

a video signal processing unit, responsive to the frequency dividing unit, for processing the input video signal and outputting the processed video signal synchronized with the frame sync signal for output; and

an audio signal processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process of the input audio signal so that a number of samples of one frame period in which the frame sync signal for output is used as a reference is equal to the predetermined number of samples;

(b) an MPEG compressing circuit for compressing the processed video signal and the processed audio signal outputted from the DV decoder by MPEG compression and forming compressed data; and

(c) a recording unit for recording the compressed data outputted from the MPEG compressing circuit.

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40. (New) A recording device according to claim 38, wherein the MPEG compressing unit executes a compressing process in accord with the reference clock outputted from the clock generator.

41. (New) A recording device according to claim 39, wherein the MPEG compressing unit executes a compressing process in accord with the reference clock outputted from the clock generator.

42. (New) A signal processing method for processing DV data including an input video signal and an input audio signal in accord with a reference clock which is asynchronous with time information for synchronization contained in the DV data, comprising the steps of:

inputting the video signal and the audio signal;

synchronizing the input video signal on a frame unit basis in response to the reference clock;

outputting the video signal which was synchronized on the frame unit basis;

sampling transforming the input audio signal in response to the reference clock on a frame unit basis different from the time information for synchronization; and

outputting the audio signal which was sampling transformed.